REMARKS

This Amendment responds to the Office Action dated January 12, 2005 in which the Examiner objected to the abstract and disclosure and rejected claims 1-4 under 35 U.S.C. §103.

Attached to this Amendment is a copy of an Information Disclosure Statement and stamped Postcard filed December 12, 2001. Applicant respectfully requests the Examiner acknowledges the Information Disclosure Statement.

Additionally, Applicant respectfully points out to the Examiner that *Asano et al.* (U.S. Patent No. 5,636,343) cited in the body of the Office Action is not cited on the Notice of References Cited (PTO-892). Applicant respectfully requests a new Notice of References Cited be provided.

As indicated above, the abstract has been amended in order to correct a minor informality. Applicant respectfully requests the Examiner approves the correction and withdraws the objection to the abstract.

As indicated above, the specification has been amended in order to correct a minor informality. Applicant respectfully requests the Examiner approves the correction and withdraws the objection to the disclosure.

As indicated above, claims 1 and 3 have been amended for stylistic reasons. The Amendment is unrelated to a statutory requirement for patentability and does narrow the literal scope of the claims.

Claim 1 claims a serial-data-communication apparatus and claims 3 claims a method of detecting a communication error in transmission and reception of serial data composed of a plurality of bits including a start bit at a head. The apparatus and method comprised an edge-detecting means, start-bit-level-inspection means

and start-bit-detection-error-notification means. The edge-detection means is for detecting a trailing edge of received data. The start-bit-level-inspection means is for recognizing the reception of the start bit of the received data based upon the detection of the trailing edge provided by the edge-detection means, and is for monitoring a bit level of the start bit to examine whether the start bit maintains a predetermined bit level. The start-bit-detection-error-notification means outputs a signal to an external circuit which indicates occurrence of an error in detecting the start bit, when any change in the bit level of the start bit is detected by the start-bit-level-inspection means.

Through the structure and method of the claimed invention a) recognizing reception of a start bit based upon detection of the trailing bit, b) monitoring the bit level of the start bit and c) outputting a signal indicating the occurrence of error in detecting the start bit when any change in the bit level is detected as claimed in claims 1 and 3, the claimed invention provides a serial-data-communication apparatus and method in which any problem relating to the start bit error is immediately discovered so that the time for recovery can be reduced. The prior art does not show, teach or suggest the invention as claimed in claims 1 and 3.

Claims 1-4 were rejected under 35 U.S.C. §103 as being unpatentable over *Setoguchi et al.* (U.S. Patent No. 4,748,643) in view of *Asano et al.* (U.S. Patent No. 5,636,343).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claims and allows the claims to issue.

Setoguchi et al. appears to disclose a start bit detecting circuit which performs accurate detection of a start bit for ensuring reliable data regenerating in a receiving circuit of a bidirectional-current, start-stop synchronization type digital signal. (col. 1, lines 5-9) FIG. 4 is a block diagram of an embodiment of the present invention, illustrating an example of the arrangement of the start bit detector for a bidirectional-current, start-stop synchronization type digital signal. FIG. 5 shows its bidirectional signal format and waveforms occurring at respective parts in the detector. Reference numeral 10 indicates a sampling pulse generator, 11 a waveform reshaper, 12 a binary phase converter, 13 a detection and start circuit (I), 14 a decision circuit (I), 15 a clock pulse generator, 16 a detection and starting circuit, (II), 17 a decision circuit (II), 18 a clock pulse generator, 19 a clock pulse selector, 20 a selector, and 21 a data regenerator. (col. 3, lines 21-33) The waveform reshaper 11 shapes the received waveform (h) from the transmission line by plus side and minus side threshold values T+ and T-, thereby converting it into plus side and minus side received signals (i) and (j). The binary phase converter 12 is set at the rise of the received signal (i) and reset at the rise of the received signal (j), whereby the signals (i) and (j) are converted into a binary bi-phase received signal (u). The detection and starting circuit (I) 13 samples the received signal (i) by the sampling clock pulses (x). Having detected a state "1" in the received signal (i) ("γ" in FIG. 5) in succession for five clock pulses (x), the detection and starting circuit 13 outputs a first detection start signal (k) and stops its generation after receiving a reset signal (not shown) from the decision circuit (I) 14 or receiving the train of signals ST0 to SP. The end of the signal reception can be decided in the following manner: For example, when the data length is fixed, clock pulses (v) are counted by a predetermined number, or

when the data length is indicated in the data, it is read out and the clock pulses (v) are counted after regenerating the data by the data regenerating circuit 21, or the stop bit is formed in a specific pattern, though not shown. (col. 3, line 51 through col. 4, line 6) The detection and start circuit (II) 16 samples the signal (j) by the clock pulses (x). Having detected the state 1 ("δ" in FIG. 5) in the signal (j) in succession for five clock pulses (x), the detection and start circuit 16 outputs a second detection start output (p) and stops its generation upon a reset output (not shown) or completion of reception of signals from the decision circuit (II) 17. (col. 4, lines 42-49) By the detection and start circuit (I) 13 or the detection and start circuit (II) 16, the start bit detection is started upon detection of the pulse width greater than the duration of five clock pulses x. (Ideally, each of the pulses "γ" and "δ" of the signals (i) and (j) has a width corresponding to 10 clock pulses (x).) When the pulse "γ" is correct in item (2), the decision circuit (I) 14 is started by the detection and start circuit (I) 13, and when it is decided by the decision circuit (I) 14 that at least two of the pulses " δ", "ε" and "η" are correct, the input signal is regarded as the start bit. Where at least two of them are incorrect, the input is regarded as noise, and at that moment the detection and start circuit (I) 13 and the clock pulse generator 15 are reset, after which the next start bit is immediately searched. In a case where the pulse "γ" is incorrect and the pulse "δ" is correct in item (2), the decision circuit (II) 17 is started, and when it is decided by the decision circuit (II) 17 that the pulses "ε" and "η" are both correct, the input is regarded as the start bit. Moreover, when either one of the two pulses is incorrect, the input is regarded as noise, and the detection and start circuit (II) 16 and the clock pulse generator 18 are immediately reset, after which the next start bit is searched immediately. That is, when the input is correct at

three or more of the four points "γ", "δ", "ε" and "η", it is regarded as the start bit. Conversely, when the input is incorrect at two or more decision points, it is regarded as noise, and the next start bit is immediately searched. (col. 5, line 41 through col. 6, line 3)

Thus, *Setoguchi et al.* merely discloses a detection and starting circuit 13 which samples a receive signal i by the sampling clock pulses x and outputs a first detection start signal (col. 3, lines 59-61, 63-64). Nothing in *Setoguchi et al.* shows, teaches or suggests a start-bit-level-inspection means for recognizing the reception of the start bit based upon the detection of the trailing edge as claimed in claims 1 and 3. Rather, *Setoguchi et al.* merely discloses a detection and starting circuit 13 which outputs a start signal when a state "1" is received in succession for five clock pulses.

Additionally, *Setoguchi et al.* merely discloses that the detection and starting circuit 13 samples a received signal to detect a state "1" in succession for five clock pulses (col. 3, lines 59-64). Nothing in *Setoguchi et al.* shows, teaches or suggests monitoring a bit level to examine whether a start bit maintains a predetermined bit level as claimed in claims 1 and 3. Rather, *Setoguchi et al.* merely detects a state of a received signal and not the bit level thereof.

Furthermore, *Setoguchi et al.* merely discloses a decision circuit 14 which decides if the input signal is a start bit when the pulse width two of three pulses are correct (col. 5, lines 47-52). Nothing in *Setoguchi et al.* shows, teaches or suggests a) outputting a signal to an external circuit and b) the output signal indicates the occurrence of error in a start bit when any change in bit level of the start bit is

detected as claimed in claims 1 and 3. Rather, *Setoguchi et al.* merely discloses determining whether the pulse width of two of three signal pulses is correct.

Asano et al. appears to disclose a microcomputer which comprises a built-in serial input-output circuit which outputs data in converting parallel data into serial data and converts input serial data into parallel data. (col. 1, lines 9-12) In a transmitting period, when discordance occurs between a signal at the R.X.D terminal and a signal at the T X D terminal, the output of the exclusive-OR circuit 1 is raised to a high level. Then the output of the D flip-flop circuit 2 is made high, and an interrupt signal is given to the CPU 101. As mentioned in the above, the discordance between the signal at the R X D terminal and the signal at the T X D terminal can be detected without comparing these signals by software. In the result, the load on the software is lightened. In other words, the time to be shared for other processes, a protocol control process, for example, can be increased, so that even if a data transfer speed is made high, the transmitting-receiving process can be executed. (col. 5, lines 13-25)

Thus, *Asano et al.* merely discloses that when discordance occurs between two signals, an interrupt signal is given to CPU (col. 5 lines 14-17). Nothing in *Asano et al.* shows, teaches or suggests outputting a signal indicating the occurrence of error in detecting a start bit when any change in the bit level of the start bit is detected as claimed in claims 1 and 3. Rather, *Asano et al.* merely discloses outputting an interrupt when a discordance between two signals is detected.

A combination of *Asano et al.* and *Setoguchi et al.* would merely suggest that when a discordance occurs between received signals I and j, to output an interrupt as taught by *Asano et al.* Thus, nothing in the combination of *Setoguchi et al.* and

Asano et al. show, teach or suggest a) recognizing reception of a start bit based upon detection of a trailing edge, b) monitoring a bit level of a start bit to maintain a predetermined bit level and c) outputting a signal indicating the occurrence of error in detecting a start bit when any change in the bit level of the start bit is detected as claimed in claims 1 and 3. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 1 and 3 under 35 U.S.C. §103.

Claims 2 and 4 depend from claims 1 and 3 and recite additional features. Applicant respectfully submits that claims 2 and 4 would not have been obvious within the meaning of 35 U.S.C. §103 over *Setoguchi et al.* and *Asano et al.* at least for the reasons as set forth above with respect to claims 1 and 3. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 2 and 4 under 35 U.S.C. §103.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time.

The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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